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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,793	12/24/2003	Katsuto Tanahashi	032206	9788

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,793	TANAHASHI ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-15* is/are pending in the application.

4a) Of the above claim(s) *15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 10/.21/2005 forms the basis for this office action. Applicant substantially amended claims 1 and 4-15, and cancelled claims 2-3 and 16-18. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1, 4-6 and 14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al (US 2003/0159644 A1) in view of prior art as admitted by Applicants ("APAA"). Yonehara et al teach a semiconductor substrate **1** ([0075] and [0113]) comprising a front face and a rear face that are both mirror-polished ([0095]), wherein said semiconductor substrate contains boron at a concentration in the range $1x10^{17} - 10^{20}\ cm^{-3}$ (see [0149]) which range overlaps the claimed range in the sub-range $10^{17} - 2x10^{17}\ cm^{-3}$. In this regard it is noted that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Yonehara also teach that a crystal layer **10** is provided on the front face ([0150]), and that a minimum value of the concentration of boron, [B] (in atoms/ cm^3) is defined for a required thickness, "t" (in μm), said required thickness being t=100 nm=0.1 μm (see [0150]) of the crystal layer that satisfies the inequality as claimed, said minimum concentration being [B]=10^{17} cm^{-3} (see [0149]), because exp(0.21x0.1) ≅ 1.021 ≤ 10^{17} / [(2.2±0.2) 10^{16}] ≅ R, wherein 4.17 ≤ R ≤ 5 within 1% accuracy.*(N.B.: please note that an upper portion of the crystalline layer 3 is porous and hence is (1) another layer and (2) not truly crystalline when taken as a whole, because the porosity destroys the translational symmetry along the lattice vectors which is a defining property of crystallinity). Yonehara et al do not necessarily teach the limitation* that said semiconductor substrate meets a criterion of "an SFQR value ≤ 70 nm as a flatness of the front face". However, as admitted by Applicants as many as 40% of all conventionally produced wafers satisfy said criterion and therefore, by rule of statistics all one of ordinary skills in the art has to do is make enough of said wafers in order to be certain to have one that satisfies said criterion. With regard to claim 14, in addition Yonehara et al teach a semiconductor element formed on the front face of said semiconductor substrate (solar battery: see Figures 16 and [0072]).

On claim 4: a maximum value of a thickness of the crystal layer 10 is defined by Yonehara to be 20 μm (see [0150]), which does satisfy the claimed inequality for a required concentration of boron [B] (in atoms/cm^3), said concentration being required to be in the interval 10^{17} - 10^{20} cm^{-3} (see [0149]), hence 10^{20} being one of all required

values, because exp (0.21x20) = exp (4.2) ≅ 66.7 ≤ 4166 ≤ 10^{20} / (2.2+0.2) x 10^{16} ≤ 10^{20} / (2.2±0.2) x 10^{16}.

On claim 5: the crystal layer 10 is a silicon crystal layer ([0078]) formed by epitaxial growth ([0149]).

On claim 6: the crystal layer is a silicon-germanium alloy crystal layer ([0078].

3. ***Claims 7-11*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara and APAA as applied to claim 2 above, and further in view of Fitzgerald (US 2002/0123167 A1). As detailed claim 2 is unpatentable over Yonehara et al in view of APAA. Neither necessarily teach the claimed layered structure of SiGe and Si. However, (a) there is a specific suggestion by Yonehara et al that a layered structure of SiGe on silicon could be used to generate stress in an SOI structure ([0411]-[0412]), while Fitzgerald teaches an SOI structure with a layered SOI composition, in particular SiGe on Si (Figure 1) for the specific purpose to enhance electron mobility (see "Background of the Invention"). *Motivation* to follow the suggestion by Yonehara et al and the teaching by Fitzgerald immediately derives from the improved electron mobility and consequent higher operational speed.

On claims 8 and 9, both Yonehara et al ([0411]-[412] and Fitzgerald ([0032] and Figures 4) teach the silicon layer to be formed in an SOI structure, i.e., inherently a structure in which the silicon crystal layer is separated by a silicon oxide layer, i.e., said semiconductor substrate is an SOI substrate wherein the crystal layer is an upper silicon crystal layer separated by a silicon dioxide layer (loc.cit.).

On claim 10: while Yonehara et al teach SIMOX as a method in the prior art for making an SOI substrate ([0006]) Applicant is reminded that the limitation of claim 10 fails to further limit the device and instead only further limits the method of making. Therefore, the further limitation defined by claim 10 fails to distinguish over the prior art.

*On claim 11:*similarly, while Yonehara et al teach bonding steps the limitation of claim 11 fails to further limit the device but instead only limits its method of making. Hence the further limitation fails to distinguish over the prior art.

4. ***Claim 12*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al as and APAA applied to claim 1 above, and further in view of Hurley (5,698,474).

As detailed above, claim 1 is unpatentable over Yonehara et al in view of APAA, neither necessarily teaching the further limitation defined by claim 12.

However, it would have been obvious to include said further limitation in view of Hurley, who, in a patent on semiconductor wafer manufacturing for integrated circuits, hence analogous art, teaches exposing the entire backside as a flat, thinned and mirror polished for the specific purpose of creating a window suitable for inspection (see title, abstract and col. 5, lines 8-12). *Motivation* for the inclusion of the teaching by Hurley in this regard in the invention by Yonehara derives from the need to inspect the quality of the result of the manufacturing process.

5. ***Claim 13*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonehara et al and APAA as applied to claim 1 above, and further in view of Steckl et al (5,759,908). As detailed above, claim 1 is unpatentable over Yonehara et al in view of

APAA. Neither necessarily teach the further limitation defined by claim 13. However, it would have been obvious to include SiC as a substrate material for an SOI in view of Steckl et al, who teach silicon carbide SOI structures (title, abstract) for the specific purpose of *inter alia* its higher breakdown voltage (see col. 1, l. 10-22). *Motivation* to replace the silicon substrate with the silicon carbide substrate derives immediately from said higher breakdown voltage.

Response to Arguments

Applicant's arguments with respect to claims 1 and 14 and dependent claims have been considered but are moot in view of the new grounds of rejection due to a reconsideration of the content of Yonehara et al, with regrets of examiner: Yonehara et al teach the non-porous portion 10 of the crystal layer 3, hence the portion that remains truly crystalline (N.B.: pores do not conform to the spatial periodicity of the crystal), to be between 100 nm = 0.1 μm and 20 μm thick, which does qualify for the crystal layer as provided on the front face and also meets the claimed semi-inequality in the final line of claim 1 as amended and the second line from below in claim 14. Furthermore, new prior art came to light over which claim 12 is rendered obvious over Hurley, who teaches the advantage of an exposed backside, flat mirror polished face for the purpose of creating a window for inspection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
December 28, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 3663).